REMARKS

Status of pending claims

Claims 1-9, 11-12, 14-18, 20-22, and 24-28 are presently pending in this patent application. None of these claims have been amended in this response. Rather, reconsideration of the final rejection is requested in light of the following comments.

Claim rejections under 35 USC 102

Claims 1-3, 5-9, 11-12, 14-18, 20-22, and 24-28 have been rejected under 35 USC 102(b) as being anticipated by Yoshiba (4,816,815). Claims 1, 16, and 22 are independent claims, from which the remaining pending claims ultimately depend. Applicant respectfully submits that as previously pending, claims 1, 16, and 22 are patentable over Yoshiba. As such, the remaining claims rejected on this basis are patentable at least because they depend from patentable base independent claims.

Claim 1 is discussed as representative of all the independent claims insofar as the present rejection is concerned. Claim 1 recites that "the display data transfer circuit [is] to *compare* pixels of the second frame buffer memory against the pixels of the first frame buffer memory to determine whether changes have been made to the pixels of the first frame buffer memory." For example, consider the following two frame buffer memories:

A	B	B
A	A	A
B	B	A

First frame buffer memory

A	B	B
B	A	B
B	B	A

Second frame buffer memory

In each of these frame buffer memories, there are nine pixels organized over three rows and three columns. In this example, each pixel can have the value A or the value B.

In relation to the example provided and in accordance with claim 1, the display data transfer circuit compares the pixels of the second frame buffer memory against the pixels of the first frame buffer memory to determine whether changes have been made to the pixels of the first frame buffer memory. In comparing the pixels of the first row of the first frame buffer memory to the pixels of the first row of the second frame buffer memory, the display data transfer circuit determines that no changes have been made, since corresponding pixels in the first and the second frame buffer memories are identical. Likewise, in comparing the pixels of the third row of the first frame buffer memory to the pixels of the first row of the second frame buffer memory, the circuit determines that no changes have been made, since corresponding pixels in the first and the second frame buffer memories are again identical.

However, still in relation to the example provided and in accordance with claim 1, in comparing the pixels of the second row of the first frame buffer memory to the pixels of the second row of the second frame buffer memory, the display data transfer circuit determines that changes have been made to the pixels in the first and third columns of the second row of the first frame buffer memory. In particular, the pixel in the first column and the second row of the first frame buffer memory is A whereas the pixel in the first column and the second row of the second frame buffer memory is B. Likewise, the pixel in the third column and the second row of the first frame buffer memory is A whereas the pixel in the third column and the second row of the second frame buffer memory is B. Thus, in accordance with claim 1, by *comparing* the pixels of the second frame buffer memory against the pixels of the first frame buffer memory, the display data transfer circuit has determined that changes have been made to the pixels in the first and third columns of the second row of the first frame buffer memory.

Applicant respectfully submits that the display data transfer circuit in Yoshiba does not *compare* pixels of the second frame buffer memory against the pixels of the first frame buffer memory to determine whether changes have been made to the pixels of the first frame buffer memory, in contradistinction to the claimed invention. The Examiner has stated that the

controller 22 of FIG. 1 in Yoshiba corresponds to the display data transfer circuit of the invention, and that column 2, lines 40-58 of Yoshiba disclose that such a controller performs the *comparing* limitation of the claimed invention. Applicant respectfully disagrees.

> Column 2, lines 40-58 of Yoshiba state in relevant part that:
>
> The control is constructed to control the first and second memories such that, in response to a command from the host machine commanding display of an image and a command from the host machine specifying that part of display data stored in the first memory which has been updated by the host machine, display data in the updated part is transferred from the first memory to the display unit to be displayed thereon and to the second memory to be stored therein, while display data in parts other than the updated part are transferred from the second memory to the display unit to be displayed thereon . . . .

On a general level, it is noted that Yoshiba does not disclose anywhere that its controller ever *compares* the display data (i.e., pixels) of the second memory against the display data (i.e., pixels) of the first memory to determine whether changes have been made to the display data of the first memory, in contradistinction to the claimed invention. For this reason alone, Yoshiba does not anticipate the claimed invention.

More specifically, the controller in Yoshiba does not, "to determine whether changes have been made to the pixels of the first frame buffer memory," actually "*compare* pixels of the second frame buffer against the pixels of the first frame buffer memory," in contradistinction to the claimed invention. Rather, the controller in Yoshiba, "to determine whether changes have been made to the pixels of the first frame buffer memory," *receives a command* from the host machine that tells the controller to which pixels changes have been made. That is, "the controller is constructed . . . such that in response to a command from the host machine . . . specifying that part of the display data stored in the first memory which has been updated by the host machine, display data in the updated part is transferred from the first memory . . . while display data in parts other than the updated part are transferred from the second memory" (Col. 2, ll. 40-58).

In other words, the controller in Yoshiba does not have to ***compare*** the display data of the second memory against the display data of the first memory to determine whether changes have

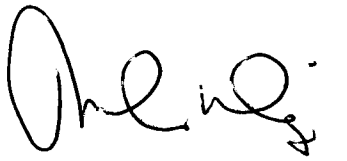
been made to the display data of the first memory, as in the claimed invention, ***because the host machine actually informs the controller whether changes have been made to the display data of the first memory***. Consider, for instance, the example presented above. While the claimed invention compares the pixels of the first memory to the pixels of the second memory to determine whether changes have been made to the pixels of the first memory, the controller in Yoshiba does not. Rather, the controller in Yoshiba is *informed by the host machine* that, for instance, the display data of the first and third columns of the second row have been changed in the first memory. No first memory-to-second memory pixel *comparison* is performed by the controller in Yoshiba to determine whether changes have been made to the first memory's pixels, and in fact it does not make sense for Yoshiba to even do this, because the host machine *informs* the controller whether changes have been made to the first memory's pixels.

Therefore, Yoshiba cannot anticipate the claimed invention. The standard for anticipation under 35 USC 102 is that every limitation of a claim must identically appear in a single prior art reference for it to anticipate the claim. (In re Bond, 15 USPQ2d 1566 (Fed. Cir. 1990)) "T]here must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention." (Scripps Clinic & Research Found. v. Genentech, Inc., 18 USPQ2d 1001, 1010 (Fed. Cir. 1991)) In the present situation, not every limitation is found identically in Yoshiba, and there is a difference between the claimed invention and Yoshiba, such that there is no anticipation.

Claim rejections under 35 USC 103

Claim 4 has been rejected under 35 USC 103(a) as being unpatentable over Yoshiba in view of Dunn (4,497,036). Claim 4 is a dependent claim, ultimately depending from claim 1, and therefore is patentable at least because claim 1 is patentable, as has been discussed above.

Respectfully Submitted,



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